



Backside Chippings Improvement through Wafer Dicing Parameter Optimization and Understanding the Anisotropic Silicon Properties

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Authors' contributions

This work was carried out in collaboration among all authors. All authors read and approved the final manuscript.

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ABSTRACT

Semiconductor Companies and Industries soar high as the trend for electronic gadgets and devices increases. Transition from “manual” to “fully automatic” application is one of the advantages why consumer adapt to changes and prefer electronic devices as one of daily answers. Individuals who admire these electronic devices often ask how they are made.

As we look inside each device, we can notice interconnected microchips commonly called IC (Integrated Circuit). These are specially prepared silicon wafers where integrated circuit are developed. Commonly, each device is composed of numerous microchips depending on the design and functionality

IC production is processed from “front-end” to “back-end” assembly. Front-end assembly includes wafer fabrication where electrical circuitry is prepared and integrated to every single silicon wafers. Back-end assembly covers processing the wafer by cutting into smaller individual and independent components called “dice”. Each dice will be placed into Leadframe, bonded with wires prior encapsulating with mold compounds. After molding, each IC will be cut through a process called singulation. Afterwards, all molded units are subjected for functional testing.

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Dice is central to each IC; it is where miniature transistor, resistor and capacitor are integrated to form complex small circuitry in microchips.

Pre-assembly (Pre-assy) stations have the first hand prior to all succeeding stations. Live wafers are primary direct materials processed in these stations. Robust work instruction and parameter must be practiced during handling and processing to avoid gross rejection and possible work-related defects.

The paper is all about the challenges to resolve and improved the backside chippings in 280um wafer thickness in mechanical dicing saw. The conventional Mechanical dicing process induce a lot of mechanical stress and vibration during the cutting process which oftentimes lead to backside chipping and die crack issues. However, backside chippings can mitigate with proper selection of parameter settings and understand the silicon wafer properties.

Keywords: Pre assembly; anisotropic silicon; wafer dicing.

1. INTRODUCTION

Continuous improvement and development have been embraced by the company designed to satisfy customer requirements. To be able to be competitive to changes, precise and robust practices are implemented to maintain good quality and reliability of the actual units produced.

In relation to the pre-assy processes, it necessarily requires improvement on chippings to intensify the die strength at the package construction, having a direct effect on package reliability and quality.

By providing standardized and workable range of parameters, chipping-related defects could be minimized, hence mitigating its effect on the overall package reliability. Also, the possibility of relaying related defects to a variety of wafer technology and succeeding packages could be eliminated.

Wafer are categorized based on what family of technology it belongs. Different set of indirect materials and parameter are standardized across every wafer technology classification. Thus, established practices are necessarily passed through within similar wafer technology to ensure positive response based on experience and data driven assessment.

Herewith documented is the experience done in pre-assembly in the improvement of backside and top side chip-out for silicon wafers done during the qualification run and evaluation.

1.1 Mechanical Wafer Dicing Sawing Process

Wafer Sawing Process involved wafer cutting into individual dice. Blade is use to singulate the silicon wafer according to the required die size

and pattern. Cutting will be done within the street width (Kerf) of the wafer pattern.

Smaller blade width versus the street width is mandatory to avoid damaging the active seal ring of the dice. Potential damage on the seal ring will result to rejection or malfunction within the unit.

The cut depth covers the total thickness of the die multiplied by the required cutting ratio appropriate with the wafer family.



Fig. 1. Mechanical wafer dicing saw process [1]

Fig. 1 shows the actual cutting of wafer to form individual die. Illustration shows that wafer is mounted to the tape to avoid “fly-off” and die movement which can lead to damage seal ring (active part) during mechanical sawing process.

1.2 Diamond Blade

Diamond blade is the primary indirect material used in the cutting of the silicon wafer. It is composed primarily of grit and bond resins (see Fig. 2). Grit is directly responsible of performing actual cutting process while Bond resins’ role is to hold the grit in placed.

Blades used in precision cutting use man made diamond grits measured by few microns. In addition Saw blades were typically used because it offers low cost process [3]

1.2 Chippings

In mechanical wafer dicing saw, one of the output responses needed to check during defining process and parameter settings is the chippings [4.5]. There were two types of

chippings on a mechanically sawn wafer based on where it is incurred namely, topside and backside chipping [6].

Topside chipping could be incurred by abrasive grit of the blade towards the surface of the die. On the other hand, Backside chipping is the cause by the cracking and the slight changes in the vertical force of the blade. These inherent characteristics of mechanical sawing could be mitigated by controlling its causes, mainly by blade, the die itself and the cutting parameters.

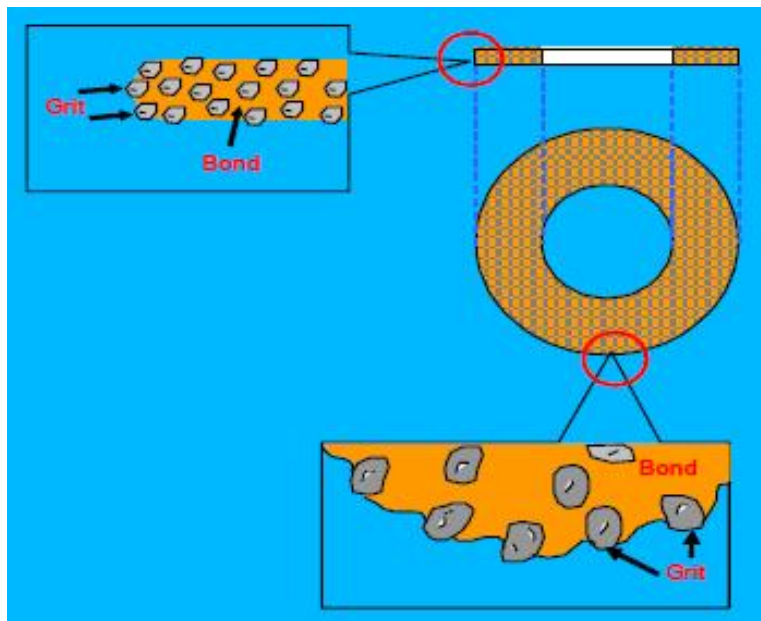


Fig. 2. Dicing blade composition [2]

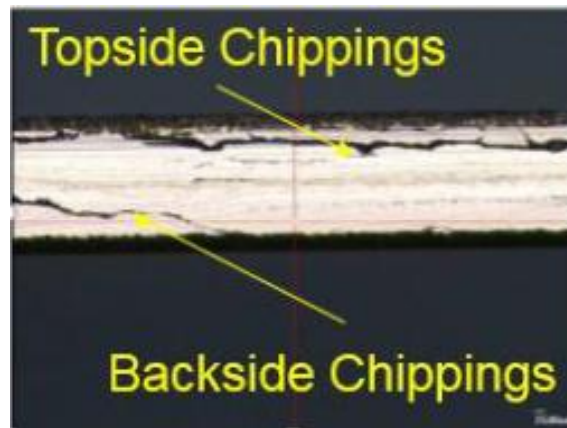


Fig. 3. Types of chippings

2. LITERATURE REVIEW

2.1 Czochralski Process

Wafer is the main carrier of microelectronics devices prior to Back-end IC manufacturing. This thin substrate, typically on a silicon monocrystalline form are fabricated using different micro fabrication process such as etching, doping/ implantation and photolithography.

The Czochralski-technique [7,8] is a method to pull a monocrystal with the same crystallographic orientation of a small monocrystalline seed crystal out of melted silicon.

A monocrystalline silicon seed crystal with the desired crystal orientation (e.g. $\langle 100 \rangle$, $\langle 110 \rangle$ or $\langle 111 \rangle$) is immersed into the melt and acts as a starting point for the crystal formation supported by the heat transfer from the melt to the already grown crystal. The seed crystal is slowly (few cm/hour) pulled out of the melt, where the pull speed determines the crystal diameter. During crystal growth, the crystal as well as the crucible counter-rotate in order to improve the homogeneity of the crystal and its dopant concentration.

At constant pulling and rotating of the seed, the formation of a mono crystalline cylindrical ingot

emerges. This cylindrical ingot, as standardized in the different semiconductor wafer fabrication sites, is in the diameter of 150, 200 and 300mm.

2.2 Miller Indices

Miller indices [10] is a group of three numbers that indicates the orientation of a plane or set of parallel planes of atoms in a crystal. If each atom in the crystal is represented by a point and these points are connected by lines, the resulting lattice may be divided into a number of identical blocks, or unit cells; the intersecting edges of one of the unit cells defines a set of crystallographic axes, and the Miller indices are determined by the intersection of the plane with these axes.

There were two flats present on a single Si wafer, primary and secondary [11]. Primary flat refers to the longest length located on the circumference of the wafer which identifies the specific crystal orientation relative to the wafer surface while the secondary flat indicates the crystal orientation and doping of the wafer.

In the back-end IC manufacturing, it is important to know the precise surface orientation because it directly affects the characteristics of certain devices. The identification of wafer flats and its correlation with the device arrays on a wafer help achieve high wafer sawing yields.

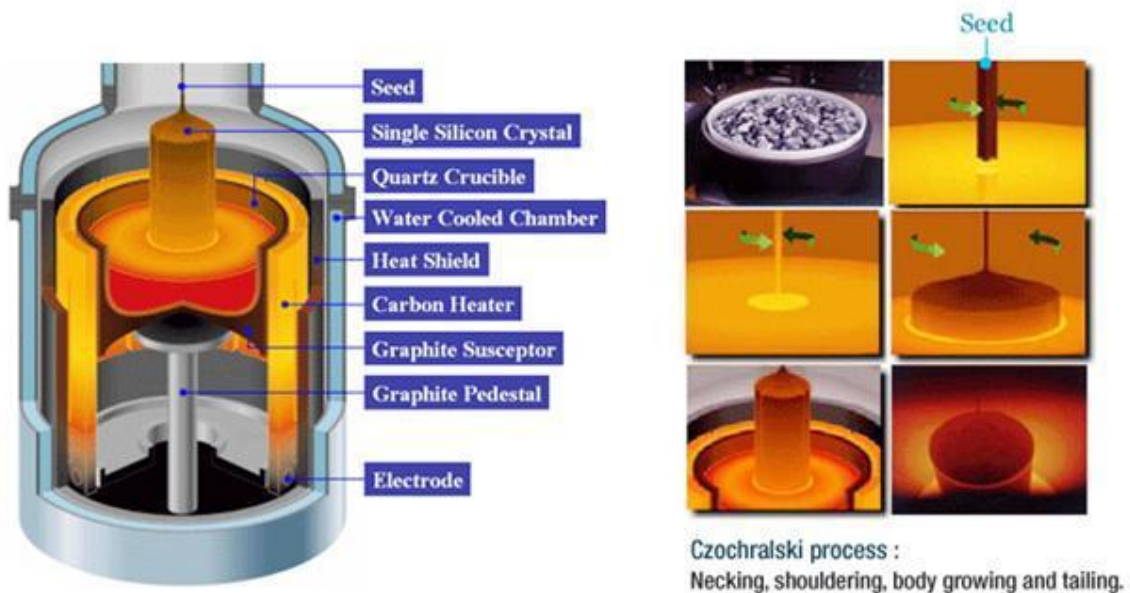


Fig. 4. Czochralski process [9]

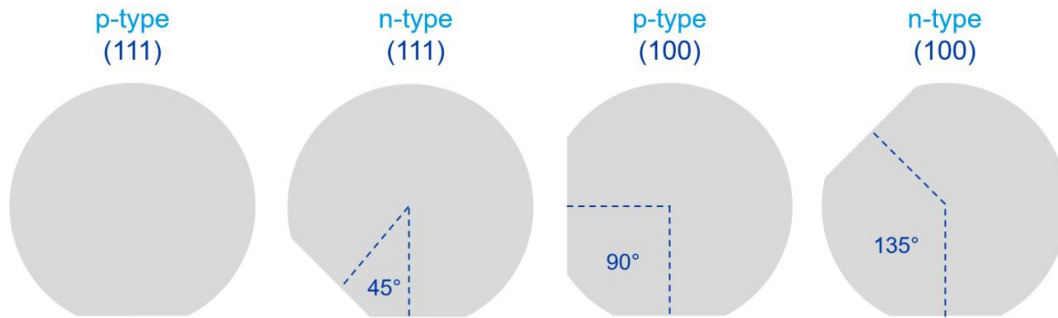


Fig. 5. Conventional Wafer Flat Identification [12]

3. EXPERIMENTATION

3.1 Materials

Wafers fabricated for motor controller device carrier on 200mm Si wafer are mounted on a normal dicing tape. All three (3) wafers are received pre-grinded at 280 μ m wafer thickness with the final die size of 2.6mm x 2.2mm.

3.2 Procedure

The experiment done is aimed to improve the sidewall backside chippings. It has been found that chipping size can be affected by several factors such as blade material (diamond concentration, grit size and bond type) and the processing parameters such as spindle speed and feed speed [13]. For this experiment, the study will focus on the process parameters. Legs could be categorized in three (3) trials: (1) higher feed speed; (2) slower feed speed and lastly (3) cutting direction or termed as cutting theta on the machine.

3.2.1 Higher feed speed

To be able to determine the response of the parameter to silicon wafer, defined parameter was considered to demonstrate the actual result.

3.2.2 Slower feed speed

Based on the result of the first trial, improvement on the backside chipping is suggested to enhance the result based on the recorded data. Backside chipping is recorded on the 2nd trial and all necessary data are documented. 1st and 2nd trial were subjected to comparative analysis to assess the improvement done on both trials.

3.2.4 Slower feed speed + Cutting theta

3rd trial was considered if ever improvement is needed based on the result of 2nd trials. Conclusion and parameter setting is discussed and all results were documented and presented.

4. RESULTS AND DISCUSSION

The experiment results were analyzed on the different Evaluation trials. Three (3) different evaluation matrices have been used to check the backside chippings response between the feed speed and the cutting theta.

4.1 Chippings Result

As per customer requirement, backside chipping should be reduced to meet the minimum range. These became a challenge with the team since mechanical sawing is prone to inherit chippings. To come up with a better solution, decision for backside chipping improvement through trials was considered.

All measurement are done using X, Y and Z scope. Standard measurement procedure is followed to determine and document the actual response of the samples. All four sides of the samples are checked. Samples are picked randomly yet covering the overall circumference of the wafer including the center. Three (3) trials are subjected for these experiment.

4.1.1 Higher feed speed result

Chipping for both backside X and Y are documented during the 1st trial. Fig. 6.a shows the maximum Z sidewall chippings acquired using higher feed speed parameter.

Shown in Fig. 6.b is the maximum backside Y chipping acquired by implementing higher feed speed parameter.

4.1.2 Slower feed speed result

Shown in Fig. 7 is the one-way analysis of low versus higher feed speed parameter. As per comparison on both 1st and 2nd trial results are not significantly different.

Based on the distribution of data in Fig. 7 backside chipping is still evident on both 1st and 2nd trial. However, variation of chippings was observed to be less on 2nd trial with slower feed speed. By decreasing the variation of all data samples as compared from 1st trial, it can be concluded that the 2nd trial has higher PPK (capability index used to identify variances within samples). Hence, reduction in chipping could be achieved by using slower feed speed parameter.

4.1.3 Cutting direction evaluation

As decided by the team, further analysis to come up with minimal chippings was performed, as guided by the actual data and evidence.

Based on the result of both 1st and 2nd trial, changing the feed speed has no significant influence in reducing the backside chippings. However, understanding the condition of the wafer could contribute to sound decision making.

During the third evaluation, the rotation of wafer during wafer sawing cutting was adjustment by certain degrees. This adjustment is due to the consideration of the miller indices of the wafer during process.

Fig. 8 shows one way analysis between three trials that backside chipping is still evident during the experiment using mechanical sawing. There are no significant difference observed on the mean of all three trials for the experiment. However, minimal variation within data samples is observed for the 3rd trial. This proves that on Trial 3, feed speed + wafer theta correction has large impact on decreasing the variation within the samples. Also, as clearly shown on Fig. 8, Trial 3 has the less chippings acquired.

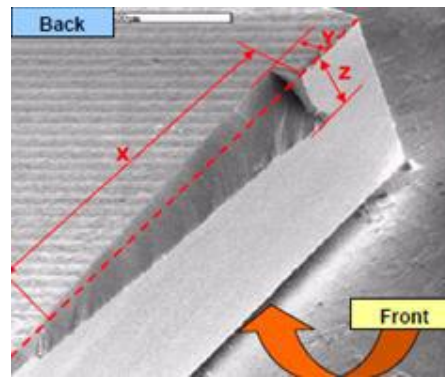


Fig. 5. Sample Photo of Backside Chippings

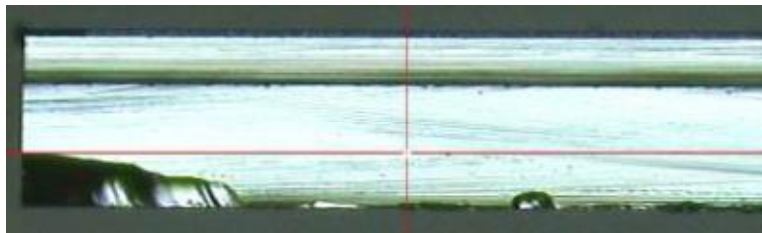


Fig. 6.a Maximum Sidewall backside chipping

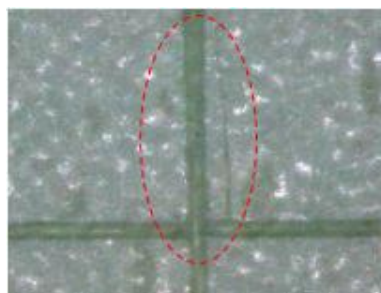


Fig. 6.b Maximum Y-axis backside chipping

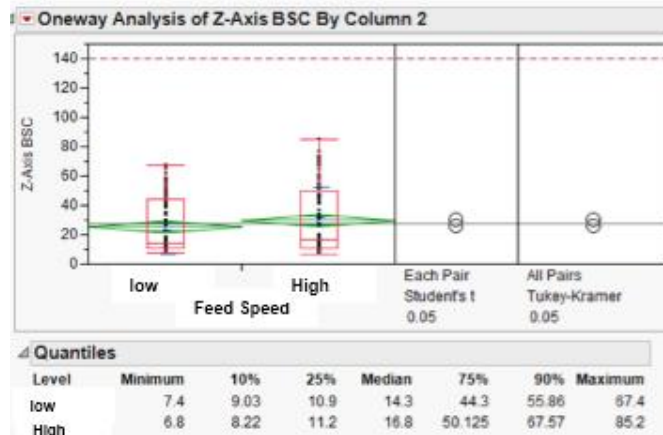


Fig. 7. ANOVA of higher vs lower feed speed. (SAS-JMP Software)

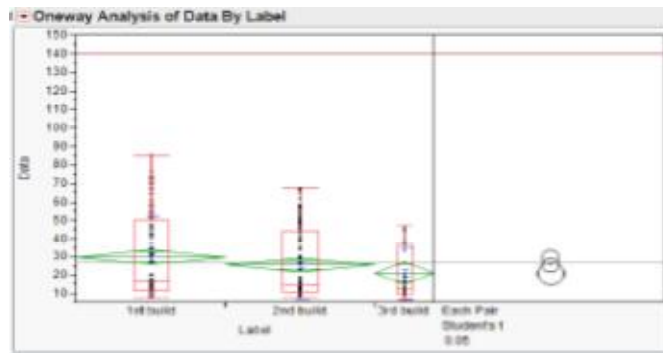


Fig. 8. ANOVA analysis of 3 trials (SAS-JMP Software)

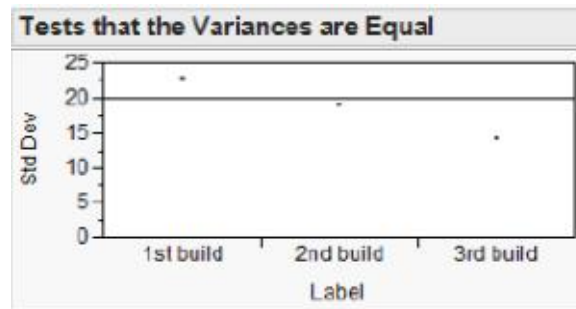


Fig. 9. Test of variance for Z backside chipping (SAS-JMP Software)

As suggested by the results summarized in Fig. 9, the optimum parameter for the test vehicle of this package is slower feed speed with wafer theta correction.

4.1.4 Revalidation

As presented earlier, chipping on mechanical sawing is inherent with the process. However, chipping can be controlled to its minimal range through optimized parameter.

Using the optimized parameter established through validation and evaluation, constant level of chipping can be acquired on all the dice within the wafer

Fig. 9 shows the comparison of standard deviation for all the three trials. In addition, Fig. 9 shows that Trial 3 has less deviation among the trials of the experiment. In addition, Trial 3 has a constant variation among all samples of the experiment.

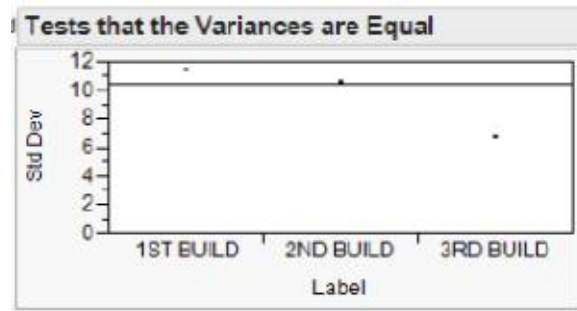


Fig. 10. Test of variance for Y backside chipping (SAS-JMP Software)

Fig. 10 shows comparison of sidewall chipping among all the three trials. Comparison among three trials shows Trial 3 has the least variation.

Fig. 10 shows comparison of Y chipping among all the three trials shows that Trial 3 has the least variation in terms of optimized feed speed + wafer theta correction.

5. CONCLUSION

Based on the presentation, chipping is observed on silicon wafers cut through the mechanical sawing process. Evaluation shows that chipping is inherent with the process.

Through evaluation and validation of the parameter, chippings can be controlled at its minimal range by deep understanding of the wafer condition, in addition to determination of the optimum parameter.

6. RECOMMENDATIONS

At the onset of development, it is highly recommended to understand a given Si wafer characteristics; specifically, it is recommended to have better understanding on the Miller indices. It is also recommended to perform evaluation and validation on different wafer packages to establish the optimum parameter.

DISCLAIMER

The products used for this research are commonly and predominantly use products in our area of research and country. There is absolutely no conflict of interest between the authors and producers of the products because we do not intend to use these products as an avenue for any litigation but for the advancement of knowledge. Also, the research was not funded by the producing company rather it was funded by personal efforts of the authors.

COMPETING INTERESTS

Authors have declared that no competing interests exist.

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